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Comparing Neural and Digital Circuits on Achieving Basic Functions Necessary for Data Processing

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Abstract: The purpose of this study is to elucidate the behavior of neural circuits. To do so, it is necessary to clarify the relationship between each neuron's inputs and outputs in order for neurons to connect in the circuit. In conventional synaptic integration theory, excitatory postsynaptic potentials (EPSPs) from multiple spines must occur almost simultaneously in order to add up them to generate an output. Thus, it is considered to be difficult for each neuron to establish synaptic integration by outputs of independent adjacent multiple neurons in the circuit. Recently, a theory that may provide a solution to this severe timing problem was proposed. The theory is that the Ca^{2+} ions retained in the spine for a long period of time polarize the neighboring highly dielectric spine-neck and dendritic fluid, resulting in an increase in membrane potential and the establishment of synaptic integration. In this study, I derived a conditional Equation for the establishment of synaptic integration that includes the effect of inhibitory neuron output, based on this theory. Based on this Equation and the morphology of neurons, I determined the circuit symbols and operation rules of neurons, and investigated to what extent a neural circuit consisting of excitatory and inhibitory neurons can reproduce the basic functions necessary for information processing compared to a digital circuit. The results showed that most of the basic functions necessary for information processing can be realized and that inhibitory neurons play important role, while there are some peculiarities as a neural circuit.

Keywords: Polarization, Dielectric Constant, Spine-Neck Capacitance, Ca^{2+}, NMDA Receptor, Synchronization

1. Introduction

1.1. Approach

In the past, most reports on neuronal connections were concerned with excitatory neurons [1], but detailed reports on inhibitory neurons have recently appeared as well. For example, it has been reported that there are many kinds of inhibitory neurons and that the output of inhibitory neurons connects with synapses of the dendrites, somas, spines, and axon terminals of the other neurons [2-6]. Thus, it seemed possible to combine excitatory and inhibitory neurons to form a neural circuit with a specific function. However, conventional synaptic integration theory, which requires almost simultaneous occurrence of EPSPs, makes it difficult to reliably activate adjacent neurons in the circuit at the required timing, and could present a significant obstacle to realize a specific function reproducibly [7-9]. Therefore, in order to reproducibly realize a specific function, a different approach is required, that is to be free from such strict temporal restrictions for inputs signals and to be able to utilize spines having a property of plasticity. Therefore, in this study, I decided to use a theory presented recently that synaptic integration is established by Ca^{2+} ions retained in the spine for a long period of time and by the spine-neck and dendritic fluid, which have extremely high dielectric constants [10-14]. This theory treats the long-term retention of Ca^{2+} ions in the spine as a long-term memory representing the fact that the spine had received output pulse previously [15-17]. And then it elucidates that the polarization of the extremely high dielectric spine-neck and dendritic fluid induced by the charges of Ca^{2+}ions in multiple spines raises membrane potential and opens the voltage-gated Na^{+} ion channel (*Note 1*) [10, 12, 18, 19]. Hereafter, I refer to this theory as the CaD synaptic integration theory which takes into account retained Ca2+ ions and fluid with an extremely high Dielectric constant [10-12]. In order to apply CaD synaptic integration theory to neural circuits, it is necessary to understand the principle of CaD synaptic integration theory, and then to clarify the conditions under which synaptic integration is established, taking into account the effects of both excitatory and inhibitory neuronal outputs.

Note 1: In neurons, the term polarization is a very confusing term. Traditionally, a neuron is said to be polarized when the difference in ionic concentration of the ionic fluid inside and outside the neuron membrane causes a potential difference between inside and outside the neuron [20-22]. On the other hand, polarization, commonly used in electromagnetism, means the polarization of the interior of any substance in proportion to the strength of the electric field and the dielectric constant of the substance. And a relative dielectric constant is the ratio of the dielectric constant of the object substance and the vacuum dielectric constant [18, 19].

1.2. Equation for the Condition of Establishment of Synaptic Integration

Based on the CaD synaptic integration theory, to understand the behavior of a neural circuit composed of excitatory and inhibitory neurons, it is necessary to understand how the neurons receiving the output of excitatory and inhibitory neurons achieve synaptic integration based on their output. According to the CaD synaptic integration theory [12], the condition for the establishment of synaptic integration is that the voltage calculated by dividing the total charge ΣQ_{Ca} of spines retaining Ca^{2+}ions by the total membrane capacitance ΣC_m of the neuron is 15 mV or higher. But 15 mV is when the resting potential is -65 mV and the threshold of the voltage gated Na^+ ion channel is -50 mV. Therefore, under this condition it is expressed as shown below.

$$V3_{Ca}=\Sigma Q_{Ca}/\Sigma C_m \geq 15mV \quad (1)$$

On the other hand, as shown in Figure 1, negative voltage $-V_{Cl}$ by the total negative charge ΣQ_{Cl} by negative Cl^- ions taken into the dendrite by the inhibitory receptors of the dendrite is expressed by the following equation [18].

$$-V_{Cl}=-V2_{Cl}-V3_{Cl}=\Sigma Q_{Cl}/Cd - \Sigma Q_{Cl}/\Sigma C_m \quad (2)$$

Therefore, the conditions for the establishment of synaptic integration, taking into account the effects of neurotransmitters from excitatory and inhibitory neurons, can be expressed by the following equation.

$$V3=V3_{Ca}-V3_{Cl}=(\Sigma Q_{Ca}-\Sigma Q_{Cl})/\Sigma C_m \geq 15mV \quad (3)$$

That is, Equation (3) means an important Equation for understanding the behavior of neural circuits.

As described in CaD synaptic integration theory, the amount by Ca^{2+} ions that each spine can retain is determined by the spine head size and the series capacitance C_s which is consisted of spine-neck capacitance C_n, the axial capacitance of the dendrite C_d and total membrane capacitance ΣC_m. However, once determined, amount of charge of Ca^{2+}ion of the spine does not affect the membrane potential V3 even if the charge move into dendrite. And, Ca^{2+} ions that have migrated into the dendrite are ejected out of the dendrite by Ca^{2+} ion pump on the dendritic membrane as excessive charge. And also Cl^- ions that entered the dendrite by inhibitory receptors are ejected by Cl^- ion pump. As a result, the concentration of each ion in the dendrite gradually returns to the concentration at the resting potential of -65 mV [20, 21].

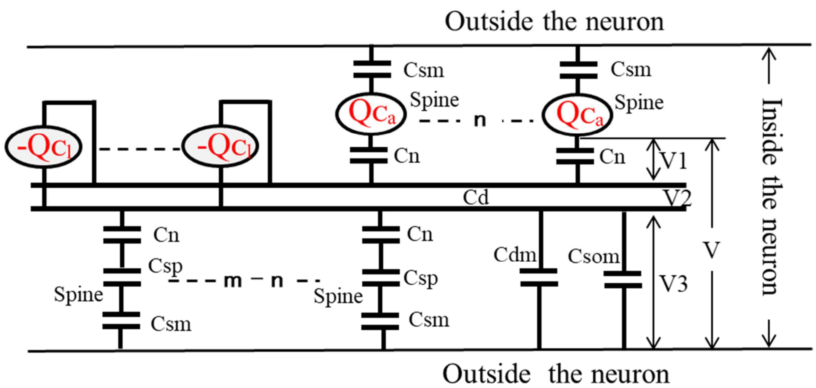

Figure 1. *Equivalent circuit of a neuron by capacitance.*

Ca^{2+} ions retained in the spine are surrounded by the spine membrane capacitance C_{sm} and the spine-neck capacitance C_n. The charge of the Ca^{2+} ions retained in the spine polarizes the medium in the spine membrane capacitance C_{sm} and the spine-neck fluid in the spine-neck capacitance C_n. The polarization of the spine-neck fluid polarizes the dendritic fluid of an axial capacitance C_d, which in turn polarizes the extracellular medium by polarizing each medium of total membrane capacity ΣC_m (Note 1). The total membrane capacitance ΣC_m is the sum of the dendritic membrane capacitance C_{dm}, the soma membrane capacitance C_{som}, and the series capacitance C_{ns} ($1/C_{ns}=1/C_n+1/C_{sp}+1/C_{sm}$) including spines that do not retain Ca^{2+} ions [18]. On the other hand, Cl^- ions incorporated into the dendrite by inhibitory receptors polarize the dendritic fluid, which in turn polarizes the extracellular medium by polarizing each medium of total membrane capacity ΣC_m. A potential is expressed at both ends of the polarization, and the potential relative to the outside of the total membrane capacitance ΣC_m is the membrane potential V3. The inside of the spine-neck and dendrites is not only ionic fluid, but only the effect of the dielectric constant of the ionic fluid has great meaning because the relative dielectric constant of ionic fluid is 10^7 to 10^8 times higher than that of other materials [10, 11, 13, 14]. Note that, excluding special substances, the relative dielectric constant of general gases, liquid and solids is 10 or less [23].

1.3. CaD Synaptic Integration Theory and Hypotheses Regarding Purging Effective Spines

Most of spines have AMPA receptors that take up Na+ ions to generate EPSPs when they receive excitatory neurotransmitters, and NMDA receptors that take up Ca^{2+} ions when the potential in the spine is increased after EPSP generation. And, Ca^{2+} ions taken into the spine by NMDA receptors cannot pass through the spine-neck and are retained in the spine [21, 22, 24, 25]. Based on this sequence of events, the CaD synaptic integration theory states that synaptic integration can be established even when there is a time interval between multiple inputs. This theory is based on the fact that Ca^{2+} ions are retained in the spine for a long time and that the electric field created by the charge of the retained Ca^{2+} ions polarizes adjacent substances in proportion to their dielectric constant [18, 19]. The dielectric constant indicates the ease of polarization of the substance, and to make it easier to understand, the relative dielectric constant, which is the ratio of the dielectric constant of an object substance and the dielectric constant of a vacuum, is often used [18.19]. Therefore, as confirmed in previous studies, since the relative dielectric constant of ion fluid in the dendrite is inversely proportional to the frequency of electric field, the relative dielectric constant of ionic fluid in neurons in a stable electric field is extremely high, ranging from 10^8 to 10^9 [11, 13, 14], therefore, its effect cannot be ignored. The CaD synaptic integration theory elucidated that the polarization of the spine-neck and dendritic fluid with extremely high relative dielectric constant generated by the Na^+ and Ca^{2+} ion charges in the spine raises the membrane potential to the threshold of the voltage-gated Na^+ ion channel and generates an action potential [12]. Such process of action potential generation is shown in the first half of Figure 2.

The latter half of Figure 2 shows that the voltage-detect Ca^{2+} ion channels (VDCCs) in the spine-neck detect the back propagation of the action potential and open the Ca^{2+} ion channels to transfer excess Ca^{2+} ions in the spine into the dendrite [26-28]. The back propagation of the action potential reaches the spine from the parent dendrite with little attenuation [12]. In the case of spine C in Figure 2, it is considered that NMDA receptors also continue to take up Ca^{2+} ion into the spine, while Ca^{2+} ions move into the dendrite in parallel. In this study, I proposed a mechanistic hypothesis in which, upon successful synaptic integration, all effective spines retaining Ca^{2+} ions are purged. This mechanism allows neurons to return to their initial state and synaptic integrate again in response to subsequent inputs, allowing for reflection and reconsideration. Without this mechanism, even after synaptic integration is established, new effective spines would increase within the neuron and continue to produce meaningless output, resulting in an increasing number of unusable neurons. We speculate that in this purging mechanism, voltage-detect Ca^{2+} ion channels (VDCCs) in the spine-neck sense the backpropagation of action potentials and open channels, allowing excess Ca^{2+} ions in the spine to move to dendrites. Therefore, as shown in Figure 2, it is thought that the generation of the EPSP of the last spine that achieved synaptic integration and the back propagation of the action potential are always close in time [26-28]. However, it is unclear how the effective spines generated by active proteins combined with Ca^{2+} ions taken up by NMDA receptors are purged [29-31]. And then, excess Ca^{2+} ions that have moved into the dendrite are ejected to the outside by the Ca^{2+} ion pump [20-22]. This flow of Ca^{2+} ions after action potential generation represents the initialization of the effective spine, which is an important *hypothesis* of this study.

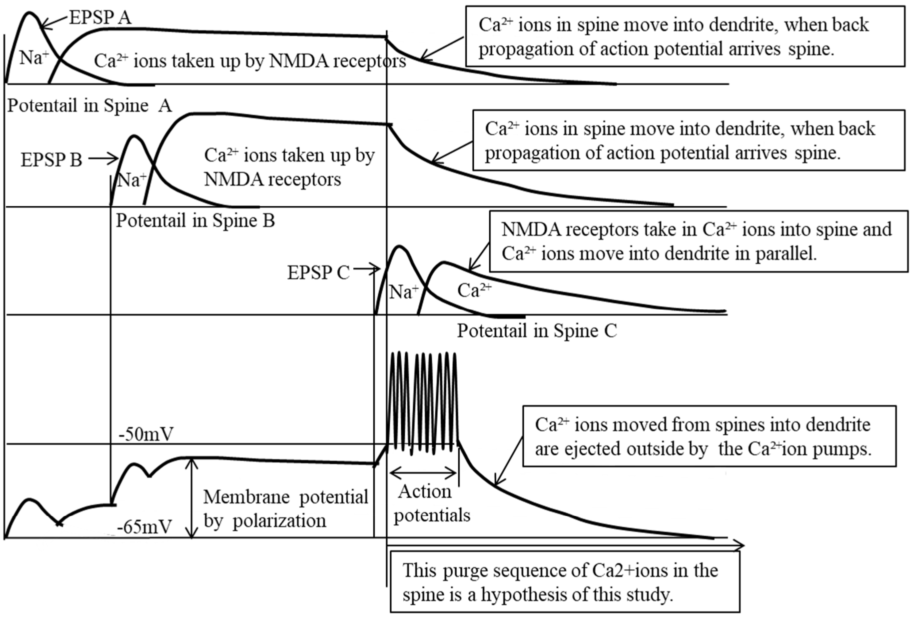

Figure 2. *Transition of spine and membrane potential.*

The voltage gated Na^+ ion channels on the axon hillock due to an increase in membrane potential caused by the charge of spine A, spine B and spine C receiving excitatory neurotransmitters generate action potential. The voltage-detect Ca^{2+} ion channels in the spine-neck open due to the back propagation of the action potential and excess C^{2+} ions in the spine are transferred to the dendrites. And then those excess Ca^{2+} ions in the dendrites are ejected outside by Ca2+ ion pump.

2. Method for Comparison

2.1. Circuit Symbol and Operation Rules of Basic Element

In order to investigate the degree to which neural circuits can reproducibly realize the basic functions required for information processing compared to digital circuits, the circuit symbol and operation rules of the basic elements must be clarified.

2.1.1. Digital Circuit

Each circuit symbol of nAND and nNAND element is shown in Figure 3 and Figure 4. But, in digital circuit, the basic element is a nNAND element. The operation rules of n NAND of the basic element are shown below [33].

i. If the input is a level, the output is also a level. And the output continues.

ii. NAND with n inputs is called nNAND as in Figure 4.

iii. The output is 0 only when all n inputs are 1s. When the input terminal is not connected, it is assumed that there is an input of 1 to the terminal.

iv. When at least one of the n inputs is 0, the output becomes 1.

The reason why the NAND element is a basic element is that the basic logic operation elements of AND, OR, and exclusive OR (EOR) can be created by combining only NAND elements, and these logic operation elements can be used to create arithmetic operation elements. In addition, a Flip Flop type memory element can be made by feeding back the output of the NAND element to the input. Therefore, LSI circuits such as microprocessors are realized by combining an enormous number of NAND gates [32].

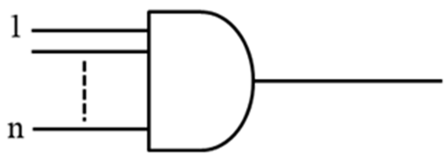

Figure 3. *Circuit symbol for nAND.*

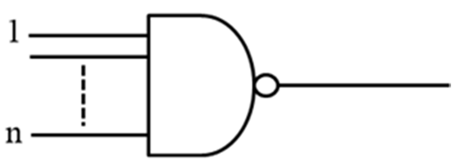

Figure 4. *Circuit symbol for nNAND.*

2.1.2. Neural Circuits

The basic elements of neural circuits are excitatory and inhibitory neurons. The circuit symbol of excitatory neuron is shown in Figure 5. The circuit symbol of inhibitory neuron is shown in Figure 6. Inhibitory neuron circuit symbol is marked with a circle at the connect point of soma and an axon to represent the release of an inhibitory neurotransmitter. In both symbols, the long line extending from the soma to the left represents the dendrite, and the short line at right angles to the dendrite represents the spine. The circles on the dendrites, spines, soma and axon terminal represent inhibitory receptors, which receive inhibitory neurotransmitters from the inhibitory neurons.

The operation rules of the basic element are shown as follow.

i. Excitatory neurons emit pulses of 1 and inhibitory neurons emit pulses of -1 when output conditions are satisfied.

ii. An input on the spine results in an effective spine with an effective number of 1. The effective number per line segment is 1 regardless of the distance from the soma (*Note 2*). A spine with a large effective number is indicated by multiple line segments connected in parallel (*Note 3*).

iii. The number displayed in the soma is the threshold number. When the sum of the effective number of effective spines equals or exceeds the threshold number, synaptic integration is established and output is emitted. The duration of output release is proportional to the amount by which the effective number exceeds the threshold number. All effective spines by Ca^{2+} ion in the neuron are purged when synaptic integration succeeds. (*Note 4*)

iv. An input by the inhibitory receptors marked with circle on dendrites result in negative effective number -1. The positive effective number of spines is subtracted by this. Inhibitory receptors marked with circle on spines and axon terminals cancel the positive effective number of those spines and axon terminals only.

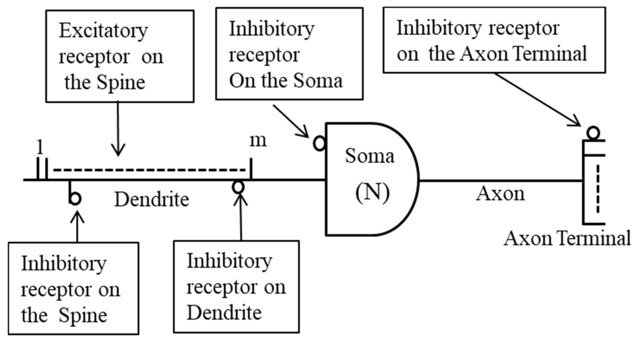

Figure 5. *Circuit symbol for excitatory neuron.*

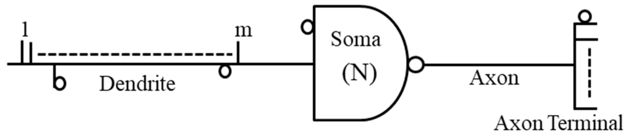

Figure 6. *Circuit symbol for inhibitory neuron.*

Note 2: As described in CaD synaptic integration theory, since the static polarization in dendrites is hardly attenuated by propagation, the contribution of spans, which are either far from the soma or close to the soma, for the establishment of synaptic integration is almost the same.

Note 3: As CaD synaptic integration theory describes, the effective number of spines is actually different for each spine because the size of the spine head and the shape of the spine-neck are different for each spine [12].

Note 4: The purge of effective spines by backpropagation of action potential is important hypothesis proposed in this study [26-28].

2.2. Comparison of Basic Elements of Digital and Neural Circuits

The basic elements of digital circuits are characterized by considering that digital circuits operate at high speed, while the basic elements of neural circuits are characterized by outputting pulses to many output destinations and receiving inputs from many neurons. Table 1 shows a comparison of both of them.

Table 1. *Comparison of basic element of digital circuit and neural circuit.*

Item	Digital circuit	Neural Circuit
Basic element	NAND	Excitatory and Inhibitory neuron
Output	High Level or Low Level	Excitatory and Inhibitory neurotransmitter
Continuity of output	Continue	Not continue (pulse)
Number of outputs	Less than 10 a)	From 1 to ten thousands b)
Number of inputs	Less than 10 a)	From 1 to ten thousands b)
Receiving place	Input terminal	Excitatory receptor on the spine (mainly) Inhibitory receptor on the dendrite, soma, spine
Operation	Logical: NAND, AND, OR, EOR Arithmetic: All type	Logical: NAND, AND, OR, EOR, Arithmetic: Add, Subtract
	Flip-flop	Retaining Ca^{2+} ion in the spine
Memory function	Set: Set and clock	Set: Opening Ca^{2+}ion channels of NMDA
	Reset: Reset and clock	Reset: Moving Ca^{2+} ion into dendrite c)

a) It reduces the number of outputs and inputs, and wiring capacitance to get higher frequency
b) It has a large number of outputs and inputs to get communication with many neurons at once.
c) This Reset condition is proposed in this study.

3. Results

3.1. Basic Logical and Arithmetic Operative Function

In a digital circuit, data for data processing is generally read from a storage device, and processed data is set in the storage device with a clock signal. Thus, data processing operations stop when the clock stops and resume when the clock restarts. Figure 7 indicates a diagram of the truth table for the basic logical operation types NAND, AND, OR, and EOR in digital circuits. In NAND, the output is 0 only when the inputs a and b are both 1s, but in the case of AND, on the contrary, the output is 1 only when both a and b are 1s. OR outputs 1 if either or both a and b is 1. EOR outputs 1 when a and b are different from each other. That is, it is the logic for knowing that two inputs are different. Figure 8 indicates the circuits of each logical operation realized only with NAND elements [33]. Figure 9 indicates a diagram of the truth table of the binary addition arithmetic operation in a digital circuit. Carry-out Co is 1 when all or any two of input Dia, Dib and carry-in Ci are 1s. 2^n carry-out Co is connected as 2^{n+1} carry-in Ci. Figure 10 indicates a part of circuit that implements an arithmetic operation unit for binary addition using only NAND elements [33].

Operation Type	Innput		Output
	a	b	c
NAND	0	0	1
	1	0	1
	0	1	1
	1	1	0
AND	0	0	0
	1	0	0
	0	1	0
	1	1	1
OR	0	0	0
	1	0	1
	0	1	1
	1	1	1
EOR	0	0	0
	1	0	1
	0	1	1
	1	1	0

Figure 7. *Truth table of digital circuit.*

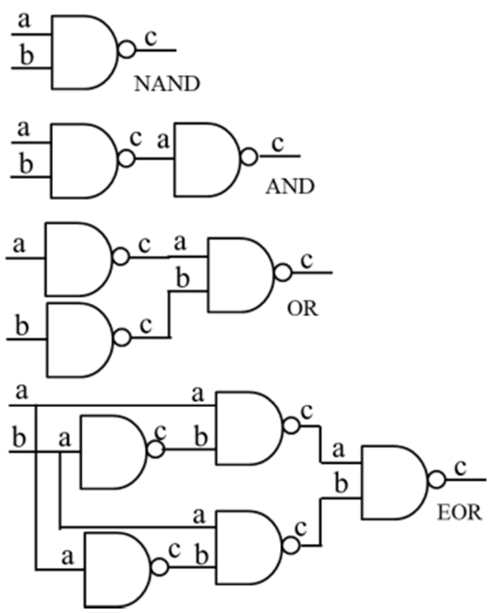

Figure 8. *Digital Circuit of logical operation.*

Binary Arithmetic Adder				
In put			Out put	
Dia	Dib	Ci	Do	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 9. *Truth table of binary add.*

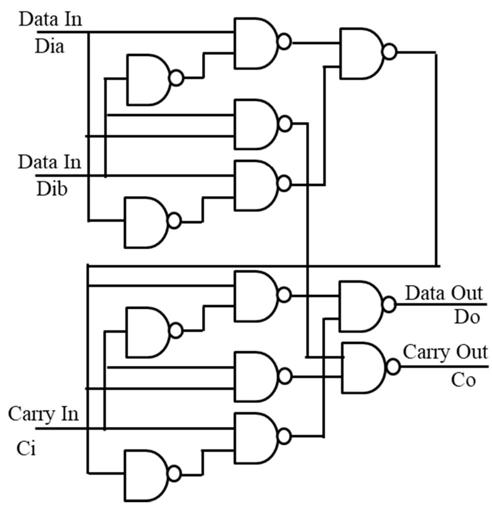

Figure 10. *Digital circuit of binary add.*

Since CaD synaptic integration theory is the base of this study, it is acceptable to have interval between input data to generate output [12]. Figure 11 indicates a diagram of the truth table for the basic operation types of neural circuits: AND, NAND, OR/Add, NOR/Subtract and EOR. AND operation is realized by an excitatory neuron, which, when both spines become effective spines, outputs 1 for a certain period of time. If the threshold number is n, 1 is output when n spines become effective spines. NAND is realized by inhibitory neuron, and the output conditions are the same as AND, but when the conditions are satisfied, it outputs -1 for a certain period of time. OR/Add is realized by excitatory neuron, where the threshold is 1, and 1 is output for a certain period when either spine a or b receives an input and becomes an effective spine. NOR/Subtract is realized by inhibitory neuron, where the threshold is 1, and -1 is output for a certain period of time when either of the spines a or b receives an input and becomes an effective spine. For Add or Subtract, when inputs a and b are received at the same time and there are two effective spines, the output is 2 or -2, that is, outputting time of output 1 or -1 is doubled. EOR is a circuit that is a combination of excitatory neurons and inhibitory neurons with threshold of 1 or -1, and outputs 1 for a certain period of time when either one of the inputs a and b becomes an effective spine. EOR is an important logical operation for recognizing that two inputs are different. Figure 12 indicates the neural circuits for each operation shown in the diagram of Figure 11. We can combine excitatory and inhibitory neurons to perform basic operations as shown in Figure 12. In this diagram, each effective number of the spine is treated as 1, but actual effective number of the spine has many kinds of value [12]. As described in the hypothesis of the previous section, all effective spines by Ca^{2+} ions retained in the spine are purged by moving Ca^{2+} ions into dendrite from the spines when back propagation of the action potential reaches to spine. Thus, new Ca^{2+} ion inputs to the spine when output is being generated are simultaneously purged into the dendrites.

Operation Type	Input		Output	Neuron Type
	a	b	c	
AND	0	0	0	Excitatory
	0	1	0	
	1	0	0	
	1	1	1	
NAND	0	0	0	Inhibitory
	0	1	0	
	1	0	0	
	1	1	-1	
OR/ Add	0	0	0	Excitatory
	0	1	1	
	1	0	1	
	1	1	2	
NOR/ Subtract	0	0	0	Inhibitory
	0	1	-1	
	1	0	-1	
	1	1	-2	
EOR	0	0	0	Excitatory/ Inhibitory
	0	1	1	
	1	0	1	
	1	1	0	

Figure 11. *Truth table of neural operation.*

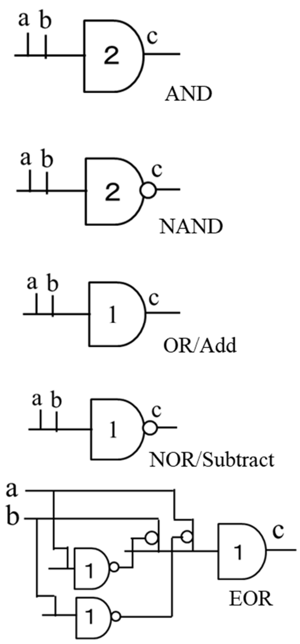

Figure 12. Neural circuit of each operation.

3.2. Encoding and Decoding Functions

Encoding and decoding functions are essential for efficient information processing. For example, 64 steps can be represented by 6 bits (2^6) by encoding them in binary exponent notation. Now, we consider an example of taste element. Theoretically, there are five taste elements: saltiness, sourness, bitterness, sweetness, and umami [34]. Assuming that each element has 64 levels of intensity, $2^6 \times 2^6 \times 2^6 \times 2^6 \times 2^6 = 2^{30}$, that is, approximately 1 billion tastes can be expressed with less than 4 bytes (30 bits). Similarly, encoding perceptions such as visual, auditory, olfactory, and tactile perceptions in exponential notation facilitates processing of the data [8, 20-22]. In the case of a computer, the data is often processed in binary exponential encoded form and decoded at the final stage. Therefore, I verified whether the neural circuit can realize the encoding/decoding function by using circuit symbols. Figure 13 is an example of a digital circuit that encodes data from 1 to 15 into 4 bits, and Figure 14 is an example of a neural circuit that performs similar encoding.

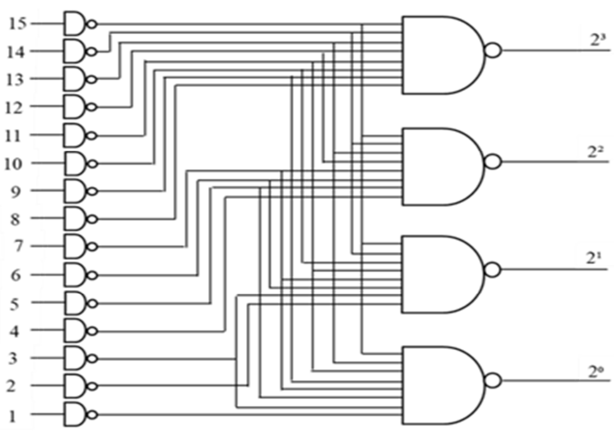

Figure 13. Encoder of digital circuit.

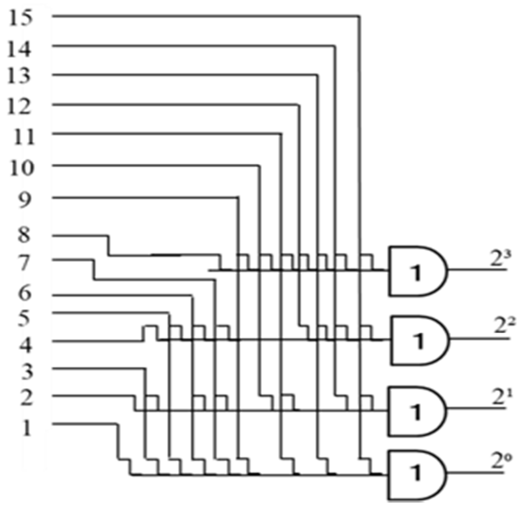

Figure 14. Encoder of neural circuit.

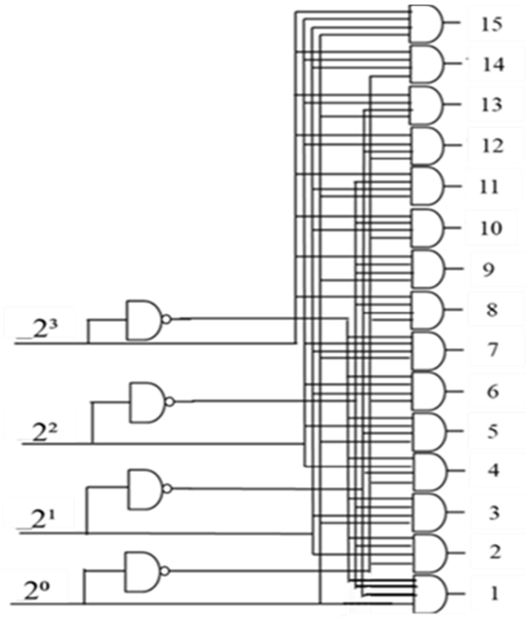

Figure 15. Decoder of digital circuit.

Figure 15 is an example of a digital circuit that decodes 4-bit encoded data to steps 1 to 15, and Figure 16 is an example of a neural circuit that performs similar decoding. In this way, it was found that data can be encoded and decoded in neural circuits as well. The brain is suitable for inputting encoded data to hippocampal pyramidal cells CA1 and CA3, which handle huge amounts of data [35, 36]. And it has been speculated that decoding functions are required to select specific motor neurons in the motor cortex [37, 38]. However, in order for the output of encoding and decoding to be stable, the input data to be encoded and decoded must be stable for some period of time. Since the data in the computer is synchronized with the clock signal, the operation result between clock signals is stable. However, in a neural network, the input data are not synchronized with each other, so the output changes according to the input. In other words, the output values of the encoding circuit and decoding circuit are not stable. Therefore, it is required that an excitatory neuron that repeatedly distributes excitatory neurotransmitters to many neurons at once is like a clock signal in order to synchronize the outputs of many neurons [39]. In each neuron, the spines that have received excitatory neurotransmitters may become effective spines. Therefore, if the neurotransmitters to the Spine C in Figure 2 is from clock neuron, the neuron may establish a synaptic integration in synchronization with the clock neuron.

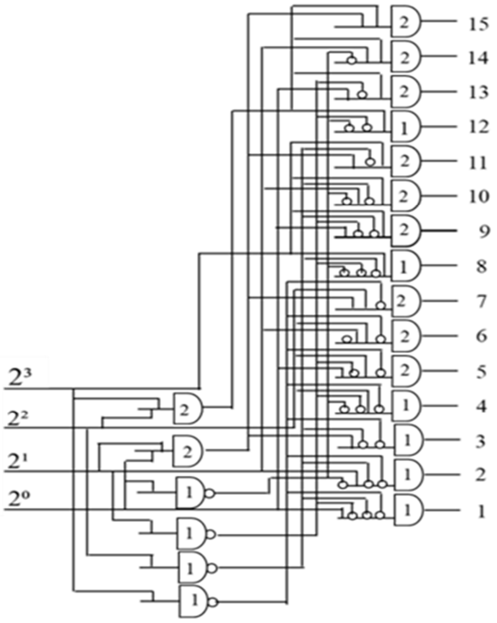

Figure 16. *Decoder of neural circuit.*

3.3. Memory Function

In a general digital computer, the data resulting from processing is retained in memory in synchronization with the clock signal. Therefore, data from the memory is synchronized with the clock signal. As a function to retain data synchronously with the clock signal, a Flip-Flop type data retention function is generally used, as shown in Figure 17. When the Set signal and the Clock signal arrive at the same time, the output of T1 becomes 0 and the output of T2 becomes 1. This is the SET state. When the Reset signal and the Clock signal arrive at the same time, the output of T4 becomes 0, the output of T3 becomes 1, and the two inputs of T2 become 1, so the output of T2 becomes 0. This is the RESET state.

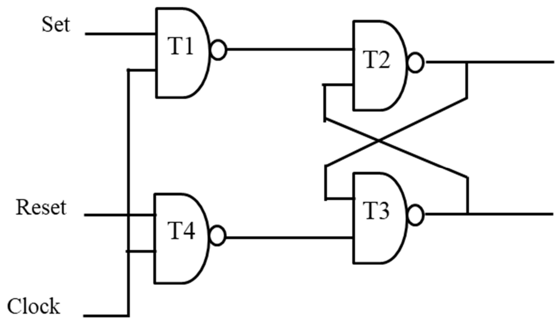

Figure 17. *Data is retained by Flip-Flop.*

On the other hand, the data retention function of neurons is realized by spine, where a huge number of spines perform the data retention function with their own time constants. As Figure 18 shows, after the spine receives excitatory neurotransmitters and AMPA receptors generate EPSP, NMDA receptors take up Ca^{2+} ions into the spine head [24, 25]. The state in which the captured Ca^{2+} ions cannot pass through the spine-neck and are retained in the spine (compartmental state) can be said to be the SET state of the data [15-17]. RESET sequence described below is a hypothesis of this study. Reset is done by the sequence that voltage-detect Ca^{2+} ion channels in the spine-neck detect the backpropagation of the action potential generated by the establishment of synaptic integration, open the channel, and cause the excess Ca^{2+} ion in the spine to move to the dendrites [26-28]. The Ca^{2+} ions that have moved into the dendrites contribute to the establishment of synaptic integration for a while, but are excreted by the Ca^{2+} ion pump of the dendrite membrane and the membrane potential drops, so the establishment of synaptic integration stops as shown in Figure 2 [20-22]. Noteworthy is the data retention method by making the spine continue to exist as an effective spine using little energy. However, how RESET is realized for the effective states produced by which Ca^{2+} ions retained in spines bind to proteins in spines, is unknown [40, 41]. There are many reports stating that each spine statistically manages its contribution to the establishment of synaptic integration in the past, which is done by reflecting the results in the internal structure and shape of the spine head and the spine-neck [42-44]. Therefore it seems that each spine can retain the quantity of Ca^{2+} ion according to its spine. That is, spine can be regarded as an advanced data retaining device that manages the amount of Ca^{2+} ions and the retention duration of Ca^{2+} ions.

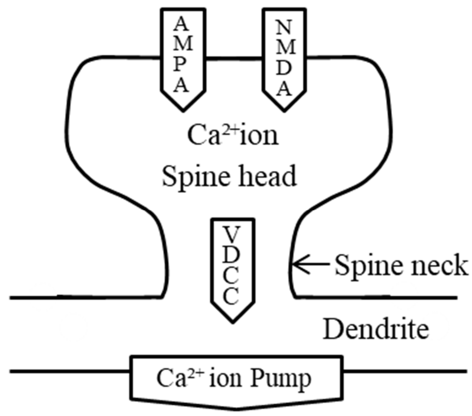

Figure 18. *Data is retained in the Spine.*

3.4. Sequence Detection Circuit

For information processing, it is often required to understand the change of events corresponding to a time sequence. For example, it is necessary to distinguish whether state A occurred at time T1 and state B occurred at the following time T2, or vice versa, state B occurred at time T1 and state A occurred at the following time T2. In a digital circuit, Figure 19 detects the occurrence of B after the occurrence of A, and Figure 20 detects the occurrence of A after the occurrence of B. In the case of a computer, when this detection circuit detects the state, it generates an interrupt to notify the program.

In a neural circuit, a similar detection can be realized with the circuits in Figure 21 and Figure 22. That is, when a neuron receives an excitatory neurotransmitter before receiving an inhibitory neurotransmitter, its synaptic integration is successful. The output is then fed back to the input and the output continues for a while. In both circuits, if the value of A is less than the value of B, A at T1 and B at T2 indicates an increase, while B at T1 and A at T2 indicates a decrease over time.

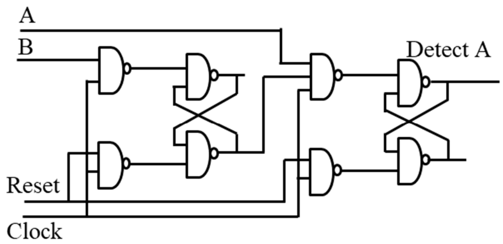

Figure 19. *A Detection digital circuit.*

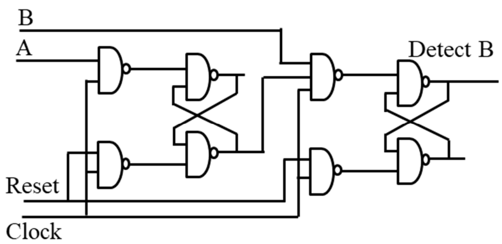

Figure 20. *B Detection digital circuit.*

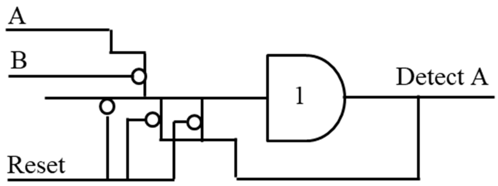

Figure 21. *A Detection neural circuit.*

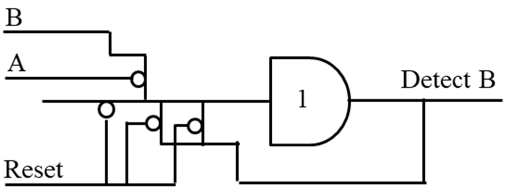

Figure 22. *B Detection neural circuit.*

3.5. Neuron as an Advanced Data Processing System

As shown in Figure 5 and Figure 6, many spines, which are advanced data retain devices, are connected to the dendrites of neurons. As described in CaD synaptic integration theory, if the number of spines connected to dendrites is m and the threshold number is n, the number of input combinations that satisfies the output condition is $_mC_n$ [12]. Some neurons such as CA1 pyramidal neurons have tens of thousands of spines. If m is 10,000 and n is 100, the number of combinations is $6.5\text{x}10^{241}$ of $_{10,000}C_{100}$. That is, it shows that AND or NAND operation can be performed for almost infinite combinations of inputs. Even if m is 1,000 and n is 10, the number of combinations is $_{1,000}C_{10}$, and calculations can be performed for a huge number of input combinations of $2.63\text{x}10^{23}$.

Furthermore, when p inhibitory receptors are present in the dendrite, the negative effective number is increased by p, so extra p positive effective spines are required. This means that the threshold number n increases to n+p. Therefore, the number of combinations is $_mC_{n+p}$. If the above m is 1,000, n is 10, and p is 5, the number of combinations is $_{1,000}C_{15}$, which is 6.88×10^{32}. That is, by increasing the number of suppressions by 5, the number of input combinations increases by more than 1 billion times. Neurons with these characteristics appear to be optimal as components of convolutional layer in deep learning mechanisms [45]. On the other hand, in a neural circuit, for example, a method of addition, subtraction, multiplication, and division operation is considered to be one combination pattern of encoded output of multiple neurons that process enormous combinations of inputs. In other words, there is no need for a logical arithmetic unit in the brain. Therefore, a single neuron having dendrites with many spines which are advanced data storage devices can be regarded as an advanced data processing system.

3.6. Circuit of Recognizing the Contour of Image (Application Example)

The first important thing in image recognition is to grasp the contour of the image. To draw a contour line, it is necessary to connect the points where the brightness of the target image changes. In order to further improve the accuracy of contour lines, it is necessary to reduce the pixel size of the image and compare the brightness of the target pixel and its neighboring pixels. When detecting that the inputs are different, it is required to determine whether or not there is a luminance difference between two pixels using an EOR operation. In practice, comparison (EOR) of the target pixel with neighboring pixels above, below, left and right is required. A comparison circuit (EOR circuit) using a digital circuit and a neural circuit will be described below. Let the plane in which the image resides be the V plane, with the x-axis horizontal and the y-axis vertical. The xy coordinates of the target pixel are V(n,n), and the coordinates of the pixels above, below, left, and right of the target pixels are V(n,n+1), V(n,n-1), V(n-1,n), V(n+1,n). The results of comparing the target pixel of the image on the V plane with the pixels on the above, below, left, and right are projected onto coordinates W(n, n) on the W plane. Figures 23 and 24 show a digital circuit and a neural circuit that compare the target pixel on the V plane with the pixels on the above, below, left, and right when target pixel of V plane is 1 as shown in Figure 25. The result of binary logic operations by digital circuits is ultimately 1 or 0. However, the result of a calculation by a neural circuit may exceed 1 because the arithmetic operation is performed with the output of excitatory neurons as 1 and the output of inhibitory neurons as -1. The following Equation (4) is the equation corresponding to the digital circuit in Figure 23. The superscript bars indicate inverts. If any of the above, below, left, or right pixels is 0, the coordinate W (n, n) is 1.

$$W(n,n)=\overline{\overline{(V(n,n)\cdot\overline{V(n,n+1)})}\cdot\overline{(V(n,n)\cdot\overline{V(n,n-1)})}\cdot\overline{(V(n,n)\cdot\overline{V(n-1,n)})}\cdot\overline{(V(n,n)\cdot\overline{V(n+1,n)})}}$$

$$=(V(n,n)\cdot\overline{V(n,n+1)}+(V(n,n)\cdot\overline{V(n,n-1)}+(V(n,n)\cdot\overline{V(n-1,n)}+(V(n,n)\cdot\overline{V(n+1,n)} \quad (4)$$

The following Equation (5) is neural circuit equation. Superscript bars indicate inhibitory neurons.

$$W(n,n)=V(n,n)+\overline{V(n,n+1)}+V(n,n)+\overline{V(n,n-1)}+V(n,n)+\overline{V(n-1,n)}+V(n,n)+\overline{V(n+1,n)}$$

$$=4xV(n,n)-(V(n,n+1)+V(n,n-1)+V(n-1,n)+V(n+1,n)) \quad (5)$$

In the case of the threshold number is 1 and the number of effective inhibitory neurons in the pixels on the above, below, left, and right is 0, 1, 2, 3, and 4, because the above equation is an arithmetic calculation, when V(n,n) is 1, the output of W (n,n) is decreased to 4, 3, 2, 1, and 0. Consider V plane of Figure 25 with square, triangle, cross, and diagonal images. Figure 26 is the W plane, which shows the results of a calculation in which the Equation (4) of the digital circuit are applied to all pixels of the V plane. Figure 27 is a W plane showing the calculation results obtained by applying Equation (5) of the neuron circuit to all pixels of the V plane. Both calculation results represent the contour of the image. The outputs of the contour (W plane) of the calculation results of the digital circuit are all 1. On the other hand, the output of the contour (W plane) of the calculation results of the neural circuit differs depending on the location of the image. In particular, the outputs for the oblique lines, corners, and tips of the V plane image are strong. As described above, the neurons perform EOR and arithmetic operations by setting the threshold number of the neuron and the effectiveness of the spine. The results are similar to the response properties of retinal circuits and complex cells visual areas [46, 47].

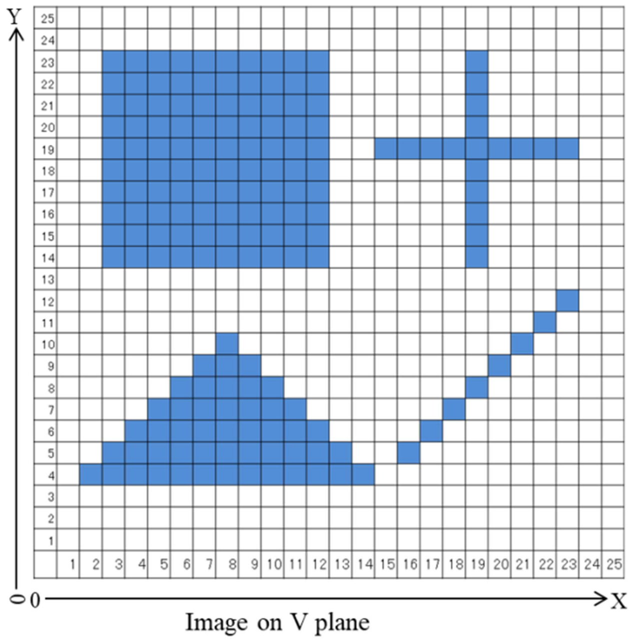

Figure 25. *Image on V plane.*

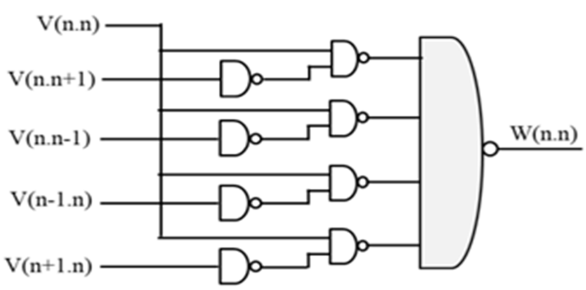

Figure 23. *Contour detect digital circuit.*

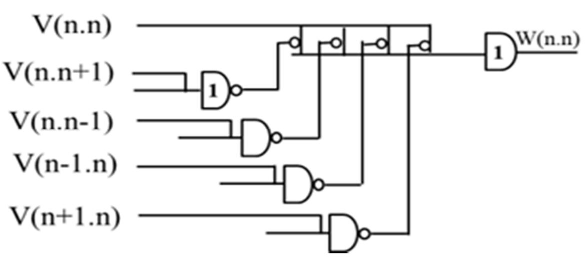

Figure 24. *Contour detect neural circuit.*

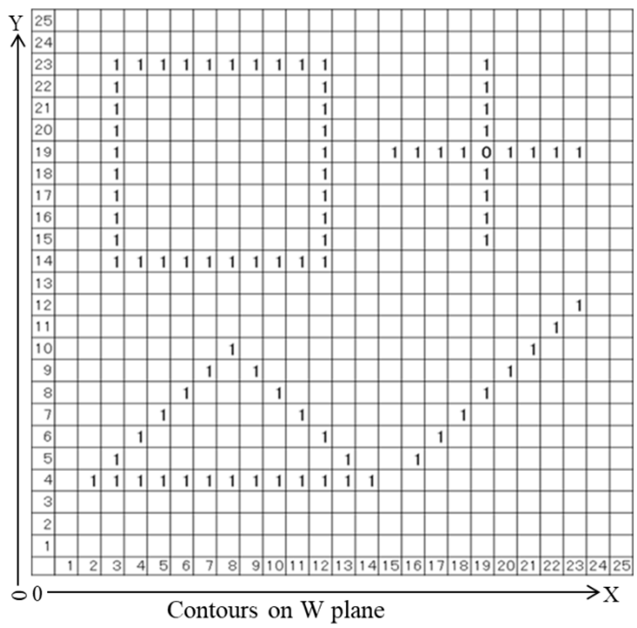

Figure 26. *Contours by digital circuit.*

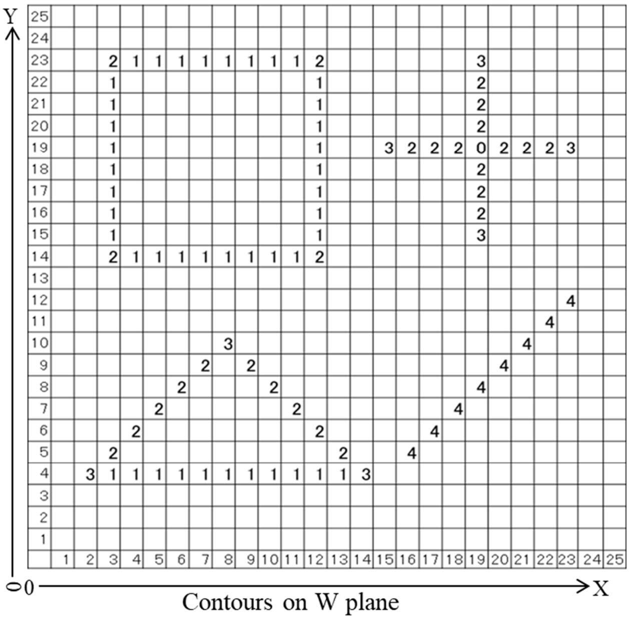

Figure 27. *Contours by neural circuit.*

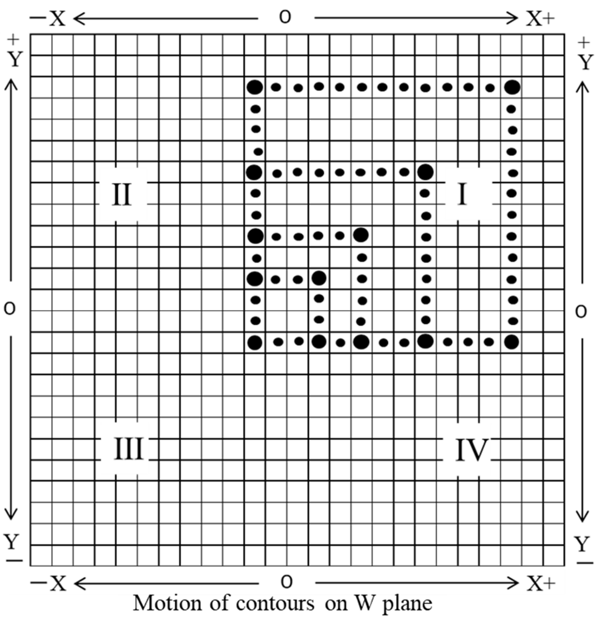

Figure 28. *Motion capture by neural circuit.*

According to the hypothesis of this study, the neurons in the components of Figure 24 purge the effective spines in the neurons immediately after outputting a pixel of plane W by an action potential generated by satisfying the output condition, so that each pixel of the contour disappears once, but the pixel of plane W is output again in response to the image of plane V. In other words, the contour of the W-plane becomes blinking contours [48, 49]. Therefore, as the image of the square on the V plane expands toward the upper right with time, its contour changes as shown in Figure 28.

3.7. Efficiently Recognition of Contour and Motion of Image in Neural Circuits (Application Example)

In the case of obtaining the contour with a digital circuit, an operation unit in the computer will be used by means of a program. In this case, data is read from the addresses of the top, bottom, left and right pixels to be compared with the target pixel in the V plane, and the EOR operation is performed on each of them according to Equation (4). Then, the results of the four EOR operations are further ORed and the result is written to the corresponding address in the W plane. By repeating this series of operations for the number of pixels on the V plane, the computer can draw the contour of Figure 26 on the W plane. Therefore, the number of program execution steps and execution time increase in proportion to the number of pixels. In order to know the movement of the image on the V plane, it is necessary to calculate the contour that changes every moment, and further calculate the expansion, reduction, and movement of that contour. Therefore, very high performance is required of the computer in order to grasp the movement of the image on the V plane in real time.

On the other hand, in the neural circuit, the output of the circuit in Figure 24, which corresponds to the number of pixels in the V plane, becomes the pixels in the W plane. Therefore, since the creation time of the W plane is only the synaptic integration time that each neuron performs in parallel, the contour can be drawn at high speed. In order to grasp the movement of the contour of the W plane, the contour shown in Figure 28 is divided into the first second, third, and fourth quadrants counterclockwise with the center of the W plane as the origin (0, 0). Then, for each quadrant, multiple neurons are prepared with different thresholds in order to add the outputs of many pixels in the quadrant in several cases. Using these neurons and the sequence detection circuit, the trend of the sum of number of pixels in each quadrant over time is analyzed to determine whether the entire image is expanding/contracting or moving vertically or horizontally. Like this case, in order to perform addition of inputs from a large number of neurons at high speed, neurons with long and narrow spine necks and small spine neck capacity (effective number of spines is less than 1/10) are suitable [9, 24]. In practice, however, it is not as simple as this because we must consider about the factor of eye movements [50].

4. Discussion

4.1. Algorithm to Understand Concretely the Behavior of Neural Circuits

To study the behavior of neural circuit, at first, based on CaD synaptic integration theory [12], the Equation (3) was derived as a form representing the influence of the outputs of excitatory and inhibitory neurons. Then, based on this Equation, the factors of morphology of neurons were taken into account, and the circuit symbols of neurons and the rules of operation of neurons were determined. This has made it possible to express the characteristics of neurons more concretely than before. That is, the threshold number is set as an index representing the total membrane capacitance ΣCm reflecting the size of the neuron and the positive effective number by effective spines and the negative effective number by inhibitory receptors are set in order to calculate total positive charges that the neuron retains. As a result, it is made clear that the neural circuit can realize functions necessary for data processing almost. In particular, it revealed the important role of inhibitory neurons. And while neural circuits are very efficient, they are also revealed to be very specific.

4.2. Analysis of Spine Morphology Using CaD Synaptic Integration Theory

Until now, many research reports have been published regarding the shape of spines. However, there has been no report that clearly analyzes how the shapes of spine heads and spine-necks contribute to the establishment of synaptic integration [51-53]. Traditionally, the resistance R of spine-necks has often been used at electric current (I=V/R) using electrons as charged particles [54, 55]. If the voltage is due to the difference in concentration of ions, the current due to electrons will not correspond. However, there are few reports from the perspective of resistance to the electric current of ions in ionic fluid as charged particles, which play an important role in neurons. Neurons skillfully utilize pumps and channels for each ion to recognize, expel and take in Na^+ ions, Ca^{2+} ions, K^+ ions and Cl^- ions. Therefore, it is required to understand from the view of ion to the spine-neck resistance. That is, when a spine-neck allows Na^+ ions to pass through but not Ca^{2+} ions, the resistance of the spine-neck can be said to be low for Na^+ ions and high for Ca^{2+} ions. However, if the Ca^{2+} ion channels in the spine-neck open and allow Ca^{2+} ions to pass through, it can be said that the spine-neck's resistance to Ca^{2+} ions becomes lower. Furthermore, as analyzed by the CaD synaptic integration theory, the charge of C^{2+} ions retained in the spine polarizes intracellular fluid, which is an ionic fluid adjacent to the charge, increases membrane potential and establishes synaptic integration [12]. In other words, neurons form a structure that takes advantage of the fact that the relative dielectric constant of K^+ ionic fluid, which has the highest concentration of 0.1M among the ionic fluid in the inner fluid of neurons, is extremely high [11, 13, 14, 23]. As CaD synaptic integration theory elucidated, the degree of contribution to the success of synaptic integration is proportional to the amount of charge of Ca^{2+} ions stored in the spine [12]. And the theory indicated that in order to store a large amount of charge in the spine, it is required to increase the size of the spine head and the capacitance of spine-neck. That is, a thick and short spine-neck is suitable for increasing the spine-neck capacitance [12]. On the other hand, since the capacitance of a long, thin spine-neck is small, electric potential in the spine increases quickly. Therefore, for the small neuron with a small threshold number, it is suitable to instantaneously get the total sum of the effective number of effective spines of a large number of spines.

4.3. The Inevitability of the Ambiguity of Neural Circuit Output

While there is no ambiguity in the output of digital circuits in logic and arithmetic operation processing, neural circuits can instantaneously perform logic and arithmetic operations on a huge number of combinations of inputs. However, a neuron circuit contains ambiguity in the result because an effective number of each spine might change dynamically according to contribution history for synaptic integration [42-44]. That is, the generation of new spines with other neurons, the size of the spine head and the spine-neck capacitance are always changing by the experience and learning [26, 43, 44]. Therefore, it seems the ambiguity by the change of the spine is inevitable for neural circuits.

4.4. Hypothesis on the Purge of Effective Spines

I proposed hypothesis of the mechanism in this study, that all effective spines by Ca^{2+} ions retained in the spine are purged when synaptic integration succeeds. By this mechanism, the neuron returns to its initial state, and it becomes possible to establish again synaptic integration for subsequent input, making reflecting and reconsidering possible. Without this mechanism, even after the establishment of synaptic integration, new effective spines would increase in the neuron and continue releasing meaningless outputs and subsequently the neurons which cannot utilize increase more and more. In this purge mechanism, I guess that voltage-detect Ca^{2+} ion channels (VDCC) on the spine-neck sense the backpropagation of the action potential and open the channel, allowing excess Ca^{2+} ions in the spine to migrate into dendrites [26-28]. However, as shown in Figure 2, it is thought that the generation of the EPSP of the last spine that achieved synaptic integration and the back propagation of the action potential are always close in time [26]. On the other hand, the back propagation of the action potential reaches the spine from the parent dendrite with little attenuation [12]. But it is unclear that how the effective spine produced by active protein combined with Ca^{2+}ions taken up by NMDA receptors are purged [29, 30].

4.5. Synchronization of the Establishment of Synaptic Integration in Multiple Neurons

It is said that there are approximately 16 billion neurons in the cerebrum [56]. If we assume that each neuron stores one bit of data, the amount of memory in the cerebrum is only 2 G bytes, which is very small. In terms of the amount of memory used by recent IT equipment, this is an amount that is instantly exhausted. However, if encoded data is used, it can be treated as an enormous amount of information. Therefore, it is assumed that data in the cerebrum is processed with encoded data and decoded at the final stage. In order to stabilize the output of encoding and decoding like a digital circuit, the input data to be encoded and decoded must be stable and synchronized with the clock signal. On the other hand, in order for neural circuits to function, synaptic integration must be established even if there is a time interval between multiple inputs. However, for encoding and decoding processing, it is required that the output from establishment of synaptic integration must be synchronized with the output of other neurons. Therefore, in order to synchronize outputs, it is necessary to have excitatory neurons that act as clocks that repeatedly release excitatory neurotransmitters to many neurons simultaneously, like a clock distribution system in a digital circuit. The spines that received excitatory neurotransmitters from the clock neurons become effective spines that may contribute to the establishment of synaptic integration. However, if there is no effective spine in the other spines in the neuron, synaptic integration cannot be established. On the other hand, in neurons whose effective number of effective spines is already close to the threshold number, synaptic integration succeeds in synchronization with EPSP generated by spines that have received neurotransmitters as shown in spine C of Figure 2. Therefore, a system for distributing clock signals for synchronization is needed to synchronize the outputs of the large number of associated neurons. However, different areas of the brain may have different clock systems with different clock frequencies and phases [39]. However, according to CaD synaptic integration theory, it is normal basic function for neuron to output synchronized with the clocks of one's own system, after receiving the outputs of multiple other clock systems as inputs. The output of a large number of neurons synchronized in this way is thought to be externally observable as an electroencephalogram.

5. Conclusion

Previous studies have elucidated that neurons take advantage of the extremely high dielectric properties of the ionic liquid inside and outside the neuron [11]. This has allowed us to elucidate that neurons achieve high conduction velocities of action potentials within motor and sensory neurons [10, 11], and highly reproducible synaptic integration by retaining the charge of Ca^{2+} ions in the spine [12]. Based on the viewpoint that neurons take advantage of the extremely high dielectric constant of ionic liquid, this study investigated the extent to which a neural circuit composed of two types of neurons, excitatory neurons that produce pulsed output and inhibitory neurons that inhibit output, can achieve the basic functions required for data processing compared with a digital circuit which uses the element having stable output. The results showed that neural circuits can realize most of the basic functions required for data processing in a way that corresponds to the properties of neurons. Underlying the properties of neurons seems to be ambiguity arising from forgetting and learning functions due to changes in spines. This study was logically derived based on previous studies from an electromagnetic viewpoint, so it needs to be confirmed by in vivo experiments.

Conflicts of Interest

The author declares no conflicts of interest.

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